Input/Output Registers

All registers for the input ports are read-only, and any writes to their memory locations will be ignored. Each register is sixteen bits in little-endian format.

Name	Ident (hex)	Length	Logic Elements	Memory (bits)
port_in	0x1001	3	208	0
port_in2	0x1002	4	266	0
port_in3	0x1003	5	320	0
port_in4	0x1004	6	320	0
port_in1_ext	0x1021	3	241	0
port_in2_ext	0x1022	4	352	0
port_in3_ext	0x1023	5	416	0
port_in4_ext	0x1024	6	461	0
port_out	0x1011	3	234	0
port_out2	0x1012	4	308	0
port_out3	0x1013	5	363	0
port_out4	0x1014	6	399	0
port_out5	0x1015	7	468	0
port_out6	0x1016	8	524	0

Register Macros

Below are the memory maps for the macros.

Address	Read/Write	Value	
Base	Read	0x1001	Ident
Base + 1	Read	0x0003	Length
Base + 2	Read	Input #1 value	Data

port_in

Address	Read/Write	Value	
Base	Read	0x1002	Ident
Base + 1	Read	0x0004	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data

port_in2

Address	Read/Write	Value	
Base	Read	0x1003	Ident
Base + 1	Read	0x0005	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data
Base + 4	Read	Input #3 value	Data

port_in3

Address	Read/Write	Value	
Base	Read	0x1004	Ident
Base + 1	Read	0x0006	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data
Base + 4	Read	Input #3 value	Data
Base + 5	Read	Input #4 value	Data

port_in4

The external input ports have a two-clock delay for input synchronization. Each register is sixteen bits in little-endian format.

Address	Read/Write	Value	
Base	Read	0x1021	Ident
Base + 1	Read	0x0003	Length
Base + 2	Read	Input #1 value	Data

port_in1_ext

Address	Read/Write	Value	
Base	Read	0x1022	Ident
Base + 1	Read	0x0004	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data

port_in2_ext

Address	Read/Write	Value	
Base	Read	0x1023	Ident
Base + 1	Read	0x0005	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data
Base + 4	Read	Input #3 value	Data

port_in3_ext

Address	Read/Write	Value	
Base	Read	0x1024	Ident
Base + 1	Read	0x0006	Length
Base + 2	Read	Input #1 value	Data
Base + 3	Read	Input #2 value	Data
Base + 4	Read	Input #3 value	Data
Base + 5	Read	Input #4 value	Data

port_in4_ext

The power-up value of all output registers is zero, 0x0000. The output port registers are read/write, with the length and identification words being read-only. Each of the registers is sixteen bits in little-endian format.

Address	Read/Write	Value	
Base	Read	0x1011	Ident
Base + 1	Read	0x0003	Length
Base + 2	Read/Write	Output #1	

port_out

Address	Read/Write	Value	
Base	Read	0x1012	Ident
Base + 1	Read	0x0004	Length
Base + 2	Read/Write	Output #1	Data
Base + 3	Read/Write	Output #2	Data

port_out2

Address	Read/Write	Value	
Base	Read	0x1013	Ident
Base + 1	Read	0x0005	Length
Base + 2	Read/Write	Output #1	Data
Base + 3	Read/Write	Output #2	Data
Base + 4	Read/Write	Output #3	Data

port_out3

Address	Read/Write	Value	
Base	Read	0x1014	Ident
Base + 1	Read	0x0006	Length
Base + 2	Read/Write	Output #1	Data
Base + 3	Read/Write	Output #2	Data
Base + 4	Read/Write	Output #3	Data
Base + 5	Read/Write	Output #4	Data

port_out4

Address	Read/Write	Value	
Base	Read	0x1015	Ident
Base + 1	Read	0x0007	Length
Base + 2	Read/Write	Output #1	Data
Base + 3	Read/Write	Output #2	Data
Base + 4	Read/Write	Output #3	Data
Base + 5	Read/Write	Output #4	Data
Base + 6	Read/Write	Output #5	Data

port_out5

Address	Read/Write	Value	
Base	Read	0x1016	Ident
Base + 1	Read	0x0008	Length
Base + 2	Read/Write	Output #1	Data
Base + 3	Read/Write	Output #2	Data
Base + 4	Read/Write	Output #3	Data
Base + 5	Read/Write	Output #4	Data
Base + 6	Read/Write	Output #5	Data
Base + 7	Read/Write	Output #6	Data

port_out6

Revisions

June 2023 – Base
March 2024 – Updated to remove extra write to port outs 1-6.