FIFO & Dual Port Memory

FIFO IN MACROS:

The first-in, first-out (FIFO) memory macros utilize Quartus macros for memory. The first two words are the identification and length words. The memory locations corresponding to the size of the FIFO memory follow these two locations. For the FIFO in memory, the memory locations are write-only. This means that a read of these locations returns a zero value. Writes to the identification and length registers are ignored. The FIFO memory uses the read-ahead function, where the data is available before a read acknowledge. The FIFO macros provide the following control signals for use within the FPGA.

fifo_d[15..0]:	Output FIFO data, where first byte appears before read request
rd_req:	An acknowledge that the data word was read.
rdfull:	Indicates that FIFO memory is full
rdempty:	Indicates that FIFO memory is empty
rdused:	Indicates the number of words available in FIFO.

For more information, see the Quartus documentation on for FIFO memory.

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
mb_fifo_in512	0x1100	258	299	4096
mb_fifo_in1024	0x1101	514	306	8192
mb_fifo_in2048	0x1102	1026	309	16384
mb_fifo_in4096	0x1103	2050	314	32768

FIFO IN Memory 16-bits

Bus writes to anywhere within the FIFO memory length are valid.

Address	Read/Write	Value	
Base	Read	0x1100	Ident
Base + 1	Read	0x0102	Length
Base + 2	Write	Writes to FIFO	
Base + 3	Write	Writes to FIFO	
. . .			
Base + 257	Write	Writes to FIFO	

Memory Map mb_fifo_in256

Address	Read/Write	Value	
Base	Read	0x1101	Ident
Base + 1	Read	0x0202	Length
Base + 2	Write	Writes to FIFO	
Base + 3	Write	Writes to FIFO	
. . .			
Base + 513	Write	Writes to FIFO	

Memory Map mb_fifo_in512

Address	Read/Write	Value	
Base	Read	0x1102	Ident
Base + 1	Read	0x0402	Length
Base + 2	Write	Writes to FIFO	
Base + 3	Write	Writes to FIFO	
. . .			
Base + 1025	Write	Writes to FIFO	

Memory Map mb_fifo_in1024

Address	Read/Write	Value	
Base	Read	0x1100	Ident
Base + 1	Read	0x0802	Length
Base + 2	Write	Writes to FIFO	
Base + 3	Write	Writes to FIFO	
. . .			
Base + 2049	Write	Writes to FIFO	

Memory Map mb_fifo_in2048

The FIFO input macros with 8-bit output have the same memory map as the 16-bit outputs. The output data is in little endian format, where the least significant byte of the first word is the first output.

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
mb_fifo_in512_16to8	0x1110	258	381	4096
mb_fifo_in1024_16to8	0x1111	514	394	8192
mb_fifo_in2048_16to8	0x1112	1026	407	16384
mb_fifo_in4096_16to8	0x1113	2050	419	32768

FIFO IN Memory 8-bit Output

FIFO OUT MACROS:

The FIFO out memory macros, provide data input to the bus. As with the FIFO in memory the first two words are the identification and length words. The memory locations corresponding to the size of the FIFO memory follow these two locations. For the FIFO out memory, the memory locations are read-only. Writes to any location within this macros memory space will be ignored. Reads past the data within the FIFO will return the last word for all additional reads. The FIFO macros provide the following control signals for use within the FPGA.

fifo_din[15..0]:	Input data to fifo
wr_req:	Data is written into fifo when high
wrempty:	Indicates FIFO memory is empty
wrfull:	Indicates FIFO memory is full
wrused:	Indicates the number of words available in FIFO

For more information, see the Quartus documentation on for FIFO memory.

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
mb_fifo_out512	0x1200	258	304	4096
mb_fifo_out1024	0x1201	514	309	8192
mb_fifo_out2048	0x1202	1026	311	16384
mb_fifo_out4096	0x1203	2050	320	32768

FIFO OUT Memory

Address	Read/Write	Value	
Base	Read	0x1200	Ident
Base + 1	Read	0x0102	Length
Base + 2	Read	Read FIFO	
Base + 3	Read	Read FIFO	
. . .			
Base + 257	Read	Read FIFO	

Memory Map mb_fifo_out256

Address	Read/Write	Value	
Base	Read	0x1201	Ident
Base + 1	Read	0x0202	Length
Base + 2	Read	Read FIFO	
Base + 3	Read	Read FIFO	
. . .			
Base + 513	Read	Read FIFO	

Memory Map mb_fifo_out512

Address	Read/Write	Value	
Base	Read	0x1202	Ident
Base + 1	Read	0x0402	Length
Base + 2	Read	Read FIFO	
Base + 3	Read	Read FIFO	
. . .			
Base + 1025	Read	Read FIFO	

Memory Map mb_fifo_out1024

Address	Read/Write	Value	
Base	Read	0x1203	Ident
Base + 1	Read	0x0802	Length
Base + 2	Read	Read FIFO	
Base + 3	Read	Read FIFO	
. . .			
Base + 2049	Read	Read FIFO	

Memory Map mb_fifo_out2048

The FIFO output macros with 8-bit input have the same memory map as the 16-bit outputs. The output data is in little endian format, where the least significant byte of the first word is the first output.

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
mb_fifo_out512_16to8	0x1210	258	321	4096
mb_fifo_out1024_16to8	0x1211	514		8192
mb_fifo_out2048_16to8	0x1212	1026		16384
mb_fifo_out4096_16to8	0x1213	2050		32768

FIFO OUT Memory 8-bit Output

DUAL PORT MEMORY MACROS:

The dual port memories grant full read/write access to the memory both within the FPGA and from the bus. Similar to the FIFO memory, the first two words are the identification and length words. The memory locations corresponding to the memory size follow these two locations. All locations are read/writeable except for identification and length, which are read-only. Due to the input registers, there is a one clock delay on reads, and the default memory values are all zeros. The dual port memory macros provide the following control signals for use within the FPGA.

wr_din[15..0]: Input data to memory
addr_in: Input address to write
wr_en: Write when high, read when low
rd_dout[15..0]: Output data from memory

For more information, see the Quartus documentation for dual port memory.

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
mb_mem_512	0x1300	258	334	4096
mb_mem_1024	0x1301	514	341	8192
mb_mem_2048	0x1302	1026	348	16384
mb_mem_4096	0x1303	2050	354	32768

Dual Port Memory

Address	Read/Write	Value	
Base	Read	0x1300	Ident
Base + 1	Read	0x0102	Length
Base + 2	Read/Write	Value 0	
Base + 3	Read/Write	Value 1	

. . .		
Base + 257	Read/Write	Value 255

Memory Map mb_mem_256

Address	Read/Write	Value	
Base	Read	0x1201	Ident
Base + 1	Read	0x0202	Length
Base + 2	Read/Write	Value 0	
Base + 3	Read/Write	Value 1	
. . .			
Base + 513	Read/Write	Value 511	

Memory Map mb_mem_512

Address	Read/Write	Value	
Base	Read	0x1202	Ident
Base + 1	Read	0x0402	Length
Base + 2	Read/Write	Value 0	
Base + 3	Read/Write	Value 1	
. . .			
Base + 1025	Read/Write	Value 1023	

Memory Map mb_mem_1024

Address	Read/Write	Value	
Base	Read	0x1203	Ident
Base + 1	Read	0x0802	Length
Base + 2	Read/Write	Value 0	
Base + 3	Read/Write	Value 1	
. . .			
Base + 2049	Read/Write	Value 2047	

Memory Map mb_mem_2048

Revisions

August 2023 – Base
March 2024 – Added FIFO out 16to8