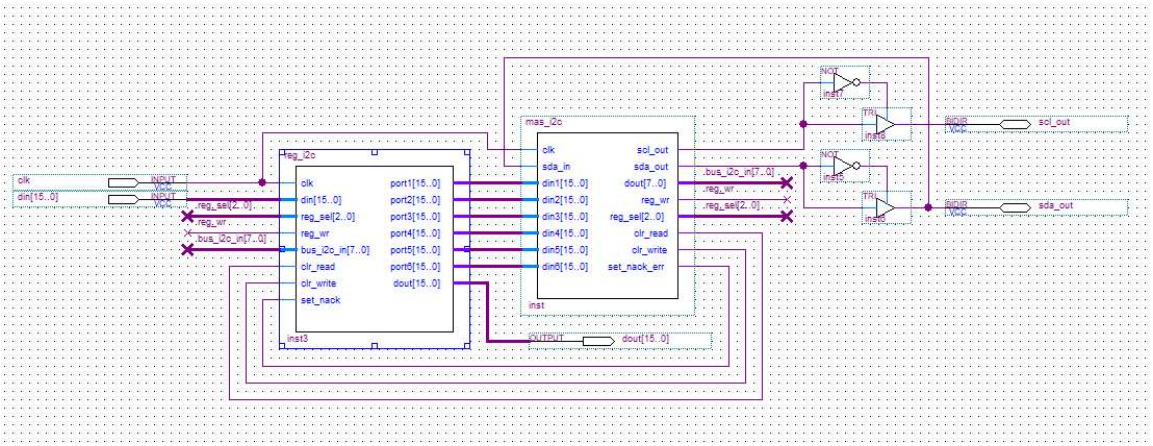
I2C Bus Master
Serial Port

I2C BUS MASTER:

This I2C controller is a bus master that support single controller mode with 7-bit addressing. The controller supports three clock speeds, without clock stretching: 100Khz, 400Khz & 1 Mhz. The controller is implemented only in logic, and supports read/write of 1 thru 8 bytes. The read mode supports a write before read, to ensure the correct data is returned. Be sure to load initial target register read address.

Macro Name	Ident	Length	Logic Elements	Memory (bits)
master_i2c	0x2001	0x0008	652	0



I2C Bus Master Block Diagram

The input/outputs from the controller are shown below:

scl_out: Bus clock (bi-directional)
sda_out: Bus data input/output (bi-directional)

Outputs required pull-up resistors.

Address	Read/Write	Value
Base	Read	ID: 0x2001
Base + 1	Read	Length: 0x0008
Base + 2	Read/Write	Register/Target Address
Base + 3	Read/Write	Control Register
Base + 4	Read/Write	Data read/write bytes 1,2
Base + 5	Read/Write	Data read/write bytes 3,4
Base + 6	Read/Write	Data read/write bytes 5,6
Base + 7	Read/Write	Data read/write bytes 7,8

Memory Map

Register, Target Address: Base +2:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	x	T	T	T	T	T	T	T

Bits 0-6: Target address, bit 7 is a don't care.
Bit 7: don't care, read/writeable.
Bits 8-15: Register address within device.

Control Register, Base +3:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	x	x	x	x	x	C	C	x	x	x	N	N	N	R	W

Bit 0: I2C bus write, '1' start write, cleared at end of write
Bit 1: I2C bus read, '1' start read, cleared at end of read
Bits 2-4: Number of bytes to read or write:
- 000 – read/write one byte
- 001 – read/write two bytes
- . . .
- 110 – read/write seven bytes
- 111 – read/write eight bytes

Bits 5-7: don't care, read/writeable.
Bits 8,9: Bus speed:
- 00 – Bus speed 100Khz
- 01 – Bus speed 400Khz
- 10 – Bus speed 1Mhz
- 11 – Bus speed 1Mhz

Bits 10-14: don't card, read/writeable.
Bit 15: ACK error, only set in hardware, cleared by user.

When bits 0 and 1 are both cleared the controller waits for next read/write.

For data writes, the data in register base+4 thru base +7 are used for the data writes. On a bus read, the base+4 thru base+7 registers are filled with the read data. Once the read bit 1 is cleared the data is valid.

Control Register, Base +4:

Bits 15 to 8	Bits 7 to 0
Byte 2	Byte 1

Control Register, Base +5:

Bits 15 to 8	Bits 7 to 0
Byte 4	Byte 3

Control Register, Base +6:

Bits 15 to 8	Bits 7 to 0
Byte 6	Byte 5

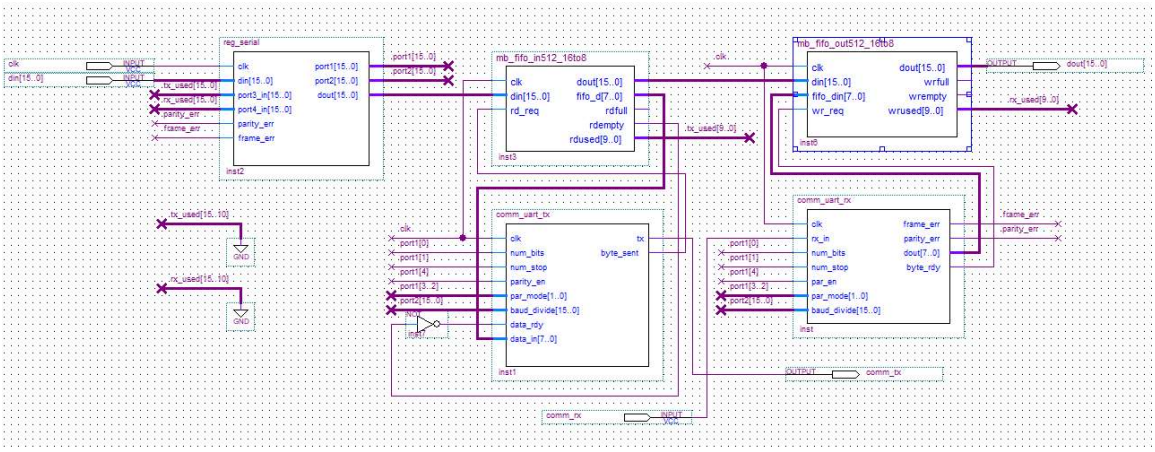
Control Register, Base +7:

Bits 15 to 8	Bits 7 to 0
Byte 8	Byte 7

SERIAL PORT:

This serial port controller supports 7,8 bits, 1,2 stop bits and parity. The input and output are buffered with 512 bytes of memory.

Macro Name	Ident	Length	Logic Elements	Memory (bits)
comm_uart	0x2002	0x020A	1079	8192



Serial Port Block Diagram

The input/outputs from the controller are shown below:

comm_rx: Receive serial port input
comm_tx: Transmit serial port output

Address	Read/Write	Value
Base	Read	ID: 0x2002
Base + 1	Read	Length: 0x0006
Base + 2	Read/Write	Control register
Base + 3	Read/Write	Baud Rate register
Base + 4	Read/Write	Transmit FIFO used
Base + 5	Read/Write	Receive FIFO used
Base + 6	Read	ID: 0x1110
Base + 7	Read	Length: 0x0102
Base + 8	Write	Transmit write FIFO
Base + 9	Write	Transmit write FIFO
. . .		
Base + 263	Write	Transmit write FIFO
Base + 264	Read	ID: 0x1200

Base + 265	Read	Length: 0x0102
Base + 266	Read	Receive read FIFO
Base + 267	Read	Receive read FIFO
. . .		
Base + 521	Read	Receive read FIFO

Memory Map

Register, Control: Base +2:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F	P	x	x	x	x	x	x	x	x	x	P	P	P	S	B

Bit 0: Number of bits: ‘0’-8 bits, ‘1’- 7 bits
Bit 1: Number of stop bits: ‘0’-1 stop bit, ‘1’- 2 stop bits
Bits 2-3: Parity Mode:

00 – space, parity always zero.
01 – mark, parity always 1.
10 – even parity
11 – odd parity

Bits 5: Parity enable: ‘0’-disabled, ‘1’-enabled
Bits 6-13: don’t care, read/writeable.
Bit 14: Parity error, only set in hardware, cleared by user.
Bit 15: Framing error, only set in hardware, cleared by user.

Baud rate register, Base +3:
Sets the baud rate of the serial port.

Baud rate = 50Mhz / (Baud rate register +1)
9,600 baud, register = 0x1457
38,400 baud, register = 0x0515
57,600 baud, register = 0x0363
115,200 baud, register = 0x01B1
230,400 baud, register = 0x00D8

Transmit FIFO used, Base +4:
The number of bytes in the FIFO from 0-512. The write is a word, so only up to 256 words maybe written to the memory.

Receive FIFO used, Base +5:
The number of bytes in the FIFO from 0-512. The read is a word, so only up to 256 words maybe read from the memory.

Revisions

March 2024 – Base