Ethernet
ACN E131

ETHERNET WRITE ONLY MACRO:

This Ethernet macro is based on the digital multiplexed (DMX) lighting standard, ACN E131. The macro provides a high speed low FPGA usage interface option for non critical applications. The DMX standard provides for up to 512 bytes of data per UDP packet as well as well as 63999 broadcast internet protocol (IP) addresses. This protocol is compatible with open source lighting control software Xlights and Vixen lights.

https://xlights.org/
https://www.vixenlights.com/

Macro Name	Ident (hex)	Length	Logic Elements	Memory (bits)
acn131_rx	0xFFF1	4	491	16384

Ethernet ACN E131 macro

ADDRESS MAPPING:

This macro provides for addressing of all 65535 word addresses within the FPGA magic bus. Each IP address corresponds to 256 words of bus space as shown below. The UPD port used for this standard is 5568, and the data byte order is little endian.

IP Address	Address Space	Comment
239.255.0.0		Reserved
239.255.0.1	0-255	Low memory
239.255.0.2	256-511	
239.255.0.3	512-767	
. . .		
239.255.1.254	64768-65023	
239.255.1.255	65024-65279	
239.255.2.0	65280-65535	High Memory
239.255.2.1		Not used, ignored
. . .		Not used, ignored

239.255.249.255		Not used, ignored
239.255.250.0		Reserved
. . .		Reserved
239.255.255.255		Reserved

Magic Bus Address Conversion

Byte order examples:

IP Address	Byte	Bus Address space
239.255.1.1	0	0x0000 LSB
239.255.1.1	1	0x0000 MSB
239.255.1.1	2	0x0001 LSB
239.255.1.1	3	0x0001 MSB
. . .		
239.255.1.2	0	0x256 LSB
239.255.1.2	1	0x256 MSB
239.255.1.2	2	0x257 LSB

Byte Order Example

Revisions

November 2023 – Base