16-Bit Pulse Width Modulator and Delta Sigma Digital to Analog Converter

Both of these modules are designed to connect to one 16-bit output port.

16-Bit Pulse Width Modulator PWM):

Macro Name	Ident	Length	Logic Elements	Memory (bits)
pwm16_ctrl	NA	NA	67	0

This outputs a pulse width asserted for a count as defined by the 16-bit input register value. There are five input parameters that setup the timing of the PWM.

clk_divide: The count divider for the system clock (50 Mhz nominally). PWM clock = 50Mhz/Divider. For example, a clock divide of 50 creates a PWM clock rate of 1Mhz. (1-65535, zero is not valid.)

period_cnt: Number of PWM clocks in a cycle (1-65535).

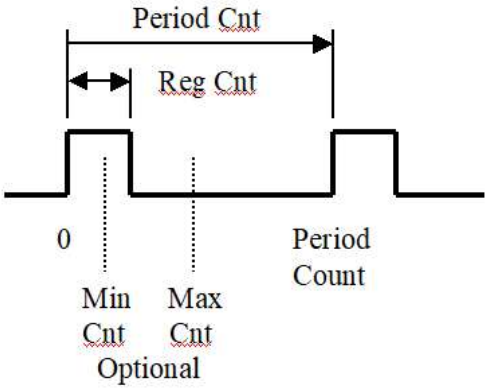
min_count: Minimum input resister PWM count, a register input less than this value will be set to this value. Set to 0 if not used.

max_count: Maximum input resister PWM count, a register input greater than this value will be set to this value. Set to 65535 if not used.

invert_output: Inverts the output pulse. “0” results in asserted high output, “1” resusts in an asserted low output.

pwm_cnt_in: The PWM will be asserted at “0” until this count, unless overridden by min/max count.

The timing of the macro is shown in the diagram below.



PWM TIMING

Delta Sigma Digital to Analog Converter:

Macro Name	Ident	Length	Logic Elements	Memory (bits)
dac_deltasig	NA	NA	52	0

The delta sigma converter uses pulse width modulation to output an analog signal on a digital pin. It is expected that the output signal will have some analog filtering. There is one parameter input along with the register input as shown below.

nbits: Selects the number of digital to analog bits equivalent for the input/output signal.

din: The signed digital input to be converted to an analog equivalent on the dout pin.

Revisions

September 2023 – Base