Pixel Controllers

All memory controllers use a first-in, first-out (FIFO) input. The controller starts outputting when the first item is loaded into memory and stops when the FIFO memory is empty. The controller does not check for memory overflow or underflow. It is the responsibility of the software to delay appropriately and ensure that the FIFO memory is cleared before starting the next output packet. The data input to the controllers is little-endian, with the least significant bit (LSB) being channel #1 and the most significant bit (MSB) being channel #2. If the data input method is slower than the output data rate, all values to the controller must be written in one message. Multiple messages are only acceptable if the input data rate is faster.

WS2811 Controller:

Macro Name	Ident	Length	Logic Elements	Memory (bits)
mb_ws2811_mem512	0x1100	258	336	4096

The controller supports WS2811 pixels up to the size of the FIFO memory. The output timing is derived from the 50MHz system clock, and its timing is shown in the table below. A larger version of the FIFO can be used to support more output channels. Note that the controller's bit timing can be modified by adjusting the parameters for the macro.

	Clocks	Time
Period	62	1.24uS
Clock High for ‘1’	35	0.70uS
Clock High for ‘0’	18	0.36uS

WS2811 Timing

Address	Read/Write	Value	
Base	Read	0x1100	Ident
Base + 1	Read	0x0102	Length
Base + 2	Write	Data	CH1,CH2
Base + 3	Write	Data	CH3,CH4
. . .			
Base + 257	Write	Data	CH511,CH512

Address Map

DMX Controller:

Macro Name	Ident	Length	Logic Elements	Memory (bits)
mb_DMX_mem512	0x1100	258	345	4096

The controller supports standard DMX outputs with up to 512 channels. The start word, generated by the controller, is always 0x00. The timing of the different parts of the output is shown below.

	Bit Clocks	Time
Bit Rate	1	4uS
MAB	24	96uS
MAB	3	12uS

DMX Timing

Address	Read/Write	Value	
Base	Read	0x1100	Ident
Base + 1	Read	0x0102	Length
Base + 2	Write	Data	CH1,CH2
Base + 3	Write	Data	CH3,CH4
. . .			
Base + 257	Write	Data	CH511,CH512

Address Map

Renard Controller:

Macro Name	Ident	Length	Logic Elements	Memory (bits)
mb_renard_mem512	0x1100	258	359	4096

The controller can support up to 512 output channels, with a default baud rate of 115.2Kbit. To adjust the baud rate, modify the clk_cnt constant comparison value in line 71 of the Renard output controller. Note that the controller will replace special characters (0x7D, 0x7E, and 0x7F) with 0x7C.

Baud Rate	Value
115.2Kbit	0x1B2
56.6Kbit	0x364
38.4Kbit	0x516
19.2Kbit	0xA2C

Baud Rate Constants

Address	Read/Write	Value	
Base	Read	0x1100	Ident
Base + 1	Read	0x0102	Length
Base + 2	Write	Data	CH1,CH2
Base + 3	Write	Data	CH3,CH4
. . .			
Base + 257	Write	Data	CH511,CH512

Address Map

Revisions

August 2023 – Base